



5 providing an A/D converter, coupled to receive the
6 signals from the transmission medium;

7 providing a sampling clock signal at a sampling clock
8 frequency equal to the characteristic occurrence frequency of
9 received signal characteristic values;

10 sampling the received signals in the A/D converter at the
11 sampling clock frequency;

12 generating signal samples at the sampling clock
13 frequency, each signal sample being output from the A/D at a time
14 assumed to correspond to the occurrence of a signal characteristic
15 value;

16 processing each signal sample in a timing recovery
17 circuit coupled, in feedback fashion, between the output of the A/D
18 and a sampling clock input thereto;

19 determining whether the occurrence of a signal
20 characteristic value leads or lags the sampling clock signal in
21 phase; and

22 adjusting the phase of the sampling clock signal such
23 that each signal sample is output from the A/D at a time that
24 actually corresponds to the occurrence of a signal characteristic
25 value, a sampling clock phase thereby being locked to a
26 corresponding phase of a signal characteristic value.

1 146. The method according to claim 145, wherein the received
2 signals are analog signals disposed in packets, the characteristic
3 values of the analog signals defining signal peaks and signal zero
4 crossings.

147. The method according to claim 145, the packets of analog signals being divided into a first region comprising timing signals and a second region comprising data signals, the method further comprising:

sampling the received data signals in the A/D converter at the sampling clock frequency, wherein the data signals are sampled after the phase of the sampling clock signal has been locked to the phase of a signal characteristic value of the timing signals.

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148. The method according to claim 147, wherein the data signals of each packet are characterized by a plurality of analog amplitude values, the values of the analog amplitudes defining information content, the analog amplitude values of the data signals being converted to digital representations thereof by the A/D converter after the phase of the sampling clock signal has been locked to the phase of a signal characteristic value of the timing signals.

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149. The method according to claim 148, further comprising:
sampling the received data signals in the A/D converter at the sampling clock frequency;
generating data signal samples at the sampling clock frequency, each data signal sample being output from the A/D at a time assumed to correspond to the occurrence of a signal characteristic value of the data signals;
processing each data signal sample in the timing recovery circuit;

10 determining whether the occurrence of a data signal
11 characteristic value leads or lags the sampling clock signal in
12 phase; and

13 adjusting the phase of the sampling clock signal such
14 that the sampling clock phase is thereby locked to a corresponding
15 phase of a data signal characteristic value.

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150. The method according to claim 149, wherein the phase
adjustment step adjusts the phase of the sampling clock signal in
discrete amounts, and wherein the discrete amount of phase
adjustment is greater when the phase adjustment step is performed
in conjunction with the timing signals than when performed in
conjunction with the data signals.

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151. The method according to claim 147, wherein the first
packet region comprises a particular number of timing signals and
wherein the phase adjustment step is performed in operative
response to a first subset of the particular number of timing
signals.

152. In a bidirectional communication system, a method of
processing signal packets received through a multi-pair
transmission medium, the signal packets including a plurality of
signals having characteristic values occurring at a characteristic
frequency, the method comprising:

providing a sampling clock signal at a sampling clock
frequency equal to the characteristic occurrence frequency of
received signal characteristic values;

9 predicting an occurrence time corresponding to the
10 characteristic occurrence frequency of received signal
11 characteristic values;

12 sampling the received signals at the sampling clock
13 frequency and at the predicted occurrence time to thereby generate
14 signal samples at the sampling clock frequency, each signal sample
15 assumed to correspond to the occurrence of a signal characteristic
16 value;

17 processing the signal samples in high gain error
18 generator, the high gain error generator determining whether the
19 occurrence of a signal characteristic value leads or lags the
20 sampling clock signal in phase; and

21 adjusting the phase of the sampling clock signal such
22 that each signal sample is generated at a time that actually
23 corresponds to the occurrence of a signal characteristic value, the
24 sampling clock having an occurrence time locked in phase with a
25 corresponding occurrence of a signal characteristic value.

1 153. The method according to claim 152, the signals of each
2 packet being characterized by a plurality of analog amplitude
3 values, the values of the analog amplitudes defining information
4 content, the method further comprising:

5 dividing the packets of analog signals into a first
6 region comprising timing signals and a second region comprising
7 data signals; and

8 converting the analog amplitude values of the data
9 signals to digital representations thereof by an A/D converter
10 after the occurrence time of the sampling clock signal has been
11 locked to the occurrence time of a signal characteristic value of
12 the timing signals.

1 154. In a bidirectional communication system, a method of
2 processing signal packets received through a multi-pair
3 transmission medium, the signal packets including a plurality of
4 timing signals having successive amplitude peaks and zero crossings
5 occurring at a characteristic frequency, the method comprising:

6 providing a sampling clock signal at a sampling clock
7 frequency equal to the characteristic occurrence frequency of
8 received signal peaks and zero crossings;

9 predicting an occurrence time corresponding to the
10 characteristic occurrence frequency of received signal peaks and
11 zero crossings;

12 sampling the received signals at the sampling clock
13 frequency and at the predicted occurrence time to thereby generate
14 signal samples at the sampling clock frequency, each signal sample
15 assumed to correspond to the occurrence of a signal peak or zero
16 crossing;

17 processing the signal samples in high gain error
18 generator, the high gain error generator determining whether the
19 occurrence of a signal peak or signal zero crossing leads or lags
20 the sampling clock signal in phase; and

21 adjusting the phase of the sampling clock signal such
22 that each signal sample is generated at a time that actually
23 corresponds to the occurrence of a signal peak or signal zero
24 crossing, the sampling clock having an occurrence time locked in
25 phase with the occurrence of a signal peak or signal zero crossing.

1 155. The method according to claim 154, the signal packets
2 further including a plurality of data signals, wherein the data
3 signals of each packet are characterized by a plurality of analog
4 amplitude values, the values of the analog amplitudes defining

5 information content, the analog amplitude values of the data
6 signals being converted to digital representations thereof by an
7 A/D converter after the phase of the sampling clock signal has been
8 locked in phase with the occurrence of a signal peak or signal zero
9 crossing of the timing signals.

1 156. In a bidirectional communication system, a method of
2 processing signal packets received through a multi-pair
3 transmission medium, the signal packets including a plurality of
4 timing signals, each timing signal having a particular one of a
5 plurality of analog amplitude values the timing signals occurring
6 at a characteristic frequency, the method comprising:

7 providing a sampling clock signal at a sampling clock
8 frequency equal to the characteristic occurrence frequency of
9 received timing signal analog values;

10 predicting an occurrence time corresponding to the
11 characteristic occurrence frequency of received timing signal
12 analog values;

13 sampling the analog values of the received timing signals
14 at the sampling clock frequency and at the predicted occurrence
15 time to thereby generate signal samples at the sampling clock
16 frequency, each signal sample assumed to correspond to the
17 occurrence of a timing signal analog value;

18 processing the signal samples in a high gain error
19 generator, the high gain error generator determining whether the
20 occurrence of a timing signal analog value leads or lags the
21 sampling clock signal in phase; and

22 adjusting the phase of the sampling clock signal such
23 that each signal sample is generated at a time that actually
24 corresponds to the occurrence of a timing signal analog value, the

25 sampling clock having an occurrence time locked in phase with a
26 corresponding occurrence of a timing signal analog value.

1 157. The method according to claim 156, the signal packets
2 further including a plurality of data signals, each data signal
3 having a particular one of a plurality of analog amplitude values
4 thereby defining information content and occurring at a
5 characteristic frequency equal to the timing signal frequency, the
6 method further comprising:

7 predicting an occurrence time corresponding to the
8 characteristic occurrence frequency of received data signal analog
9 values;

10 sampling the analog values of the received data signals
11 at the sampling clock frequency and at the predicted occurrence
12 time to thereby generate a first signal sample at the sampling
13 clock frequency, the first signal sample assumed to correspond to
14 the occurrence of a first particular data signal analog value;

15 processing the data signals through a fully digital
16 adaptive equalizer to thereby generate a symbol representation
17 corresponding to at least a second particular data signal analog
18 value;

19 processing the first signal sample and the symbol
20 representation in a low gain error generator, the low gain error
21 generator determining whether the occurrence of a data signal
22 symbol representation leads or lags the sampling clock signal in
23 phase; and

24 adjusting the phase of the sampling clock signal such
25 that each data signal analog value is sampled at a time that
26 actually corresponds to the occurrence of a data signal analog

27 value, the sampling clock having an occurrence time locked in phase
28 with a corresponding occurrence of a data signal analog value.

1 158. In a bidirectional communication system, a method of
2 processing signal packets received through a multi-pair
3 transmission medium, each packet including timing signals, the
4 timing signals oscillating at a characteristic frequency between
5 amplitudes of +1 and -1 with zero crossings therebetween, the
6 method comprising:

7 providing an A/D converter, coupled to receive the
8 signals from the transmission medium;

9 providing a sampling clock signal at a sampling clock
10 frequency four times the oscillation frequency of the timing
11 signals;

12 sampling the received timing signals in the A/D converter
13 at the sampling clock frequency;

14 generating signal samples at the sampling clock
15 frequency, each signal sample being output from the A/D at a time
16 assumed to correspond to the occurrence of a +1 amplitude, a -1
17 amplitude or a zero crossing;

18 providing a high gain error generation circuit coupled,
19 in feedback fashion, between the output of the A/D and a sampling
20 clock input thereto;

21 processing each signal sample in the high gain error
22 generation circuit, the error circuit determining a difference
23 between a predicted time of occurrence and an actual time of
24 occurrence of an indication of a zero crossing from a +1 amplitude
25 or from a -1 amplitude and outputting a metric signal corresponding
26 to said difference; and

27 adjusting the phase of the sampling clock signal in
28 accordance with the metric signal such that each signal sample is
29 output from the A/D at a time that actually corresponds to the
30 occurrence of a +1 amplitude, a -1 amplitude or a zero crossing
31 thereby locking the sampling clock in phase with the occurrence of
32 a timing signal amplitude peak or zero crossing.

1 159. The method according to claim 158, the signal packets
2 further including a plurality of data signals, wherein the data
3 signals of each packet are characterized by a plurality of analog
4 amplitude values, the values of the analog amplitudes defining
5 information content, the analog amplitude values of the data
6 signals being converted to digital representations thereof by an
7 A/D converter after the phase of the sampling clock signal has been
8 locked in phase with the occurrence of a timing signal amplitude
9 peak or signal zero crossing.

1 160. In a multi-pair bidirectional communication system, a
2 method of operating on received signals defining signal packets,
3 each signal packet including a plurality of analog signals, the
4 method comprising:

5 providing an analog to digital (A/D) converter;
6 receiving the plurality of analog signals;
7 converting the plurality of analog signals to digital
8 signals representative thereof in the A/D converter and outputting
9 said signals;

10 providing a timing recovery circuit, the timing recovery
11 circuit coupled to the output of the A/D converter and receiving
12 the digital signals;

13 evaluating a phase characteristic of the digital signals
14 in the timing recovery circuit so as to develop timing recovery
15 signals representative of changes in a characteristic occurrence
16 frequency of the digital signals;

17 regulating a sampling clock phase and frequency in
18 accordance with the timing recovery signals; and

19 coupling the sampling clock to the A/D converter, the
20 A/D converter converting analog signals to digital signals and
21 outputting said digital signals in accordance with timing intervals
22 defined by the sampling clock.

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1 161. The method according to claim 160, wherein the multi-pair
2 bidirectional communication system comprises four unshielded
3 twisted wire pairs defining a local area network, the four pairs
4 further comprising a first pair adapted for signal transmission,
5 second and third pairs adapted for bidirectional signal
6 transmission and reception and a fourth pair adapted for reception.

1 162. The method according to claim 160, further comprising:
2 providing a automatic gain control (AGC) circuit having
3 an input coupled to receive analog signals and an output coupled to
4 the A/D converter;

5 providing an AGC control loop circuit coupled, in
6 feedback fashion, between the output of the A/D converter and the
7 AGC, the AGC control loop circuit receiving the digital signals
8 output by the A/D converter and generating a gain control signal in
9 operative response thereto; and

10 controlling the operation of the AGC circuit with the
11 gain control signal, such that the gain of the received analog

12 signals is regulated, in feedback fashion, in accordance with
13 regulated gain of the digital signals output by the A/D converter.

1 163. The method according to claim 162, further comprising:
2 encoding each of the plurality of analog signals to one
3 of three analog amplitude levels, thereby representing information
4 content;

5 recovering said information content from the digital
6 signals output from the A/D converter, after the gain of the
7 received analog signals is regulated.

8 164. In a multi-pair bidirectional communication system, a
9 method of operating on received signals defining signal packets,
10 each signal packet including a plurality of analog signals, each
11 analog signal encoded into discrete amplitude levels, thereby
12 representing information content, the method comprising:

13 providing an analog to digital (A/D) converter;

14 receiving the plurality of analog signals;

15 converting the plurality of analog signals to digital
16 signals representative thereof in the A/D converter and outputting
17 said signals;

18 providing a automatic gain control (AGC) circuit having
19 an input coupled to receive analog signals and an output coupled to
20 the A/D converter;

21 providing an AGC control loop circuit coupled, in
22 feedback fashion, between the output of the A/D converter and the
23 AGC, the AGC control loop circuit receiving the digital signals
24 output by the A/D converter and generating a gain control signal in
25 operative response thereto; and

19 controlling the operation of the AGC circuit with the
20 gain control signal, such that the gain of the received analog
21 signals is regulated, in feedback fashion, in accordance with
22 regulated gain of the digital signals output by the A/D converter.

1 165. The method according to claim 164, further comprising the
2 step of recovering said information content from the digital
3 signals output from the A/D converter, after the gain of the
4 received analog signals is regulated.

5 166. The method according to claim 165, wherein the multi-pair
6 bidirectional communication system comprises four unshielded
7 twisted wire pairs defining a local area network, the four pairs
8 further comprising a first pair adapted for signal transmission,
9 second and third pairs adapted for bidirectional signal
10 transmission and reception and a fourth pair adapted for reception.

1 167. In a multi-pair bidirectional communication system, a
2 method of operating on received signals defining signal packets,
3 each signal packet including a plurality of analog signals, each
4 analog signal encoded into discrete amplitude levels, thereby
5 representing information content, the method comprising:

6 providing an analog to digital (A/D) converter;
7 receiving the plurality of analog signals;
8 converting the plurality of analog signals to digital
9 signals representative thereof in the A/D converter and outputting
10 said signals;

11 providing a fully digital adaptive equalizer coupled to
12 receive digital signals from the output of the A/D converter;

13 adaptively equalizing the digital signals so as to
14 produce compensated digital signals representing information
15 content; and

16 recovering the information content of the digital signals
17 after the adaptive equalization step.

1 168. The method according to claim 167, further comprising:
2 providing a timing recovery circuit, the timing recovery
3 circuit coupled to the output of the A/D converter and receiving
4 the digital signals;

5 evaluating a phase characteristic of the digital signals
6 in the timing recovery circuit so as to develop timing recovery
7 signals representative of changes in a characteristic occurrence
8 frequency of the digital signals;

9 regulating a sampling clock phase and frequency in
10 accordance with the timing recovery signals; and

11 coupling the sampling clock to the A/D converter, the
12 A/D converter converting analog signals to digital signals and
13 outputting said digital signals in accordance with timing intervals
14 defined by the sampling clock.

1 169. The method according to claim 168, further comprising:
2 providing a automatic gain control (AGC) circuit having
3 an input coupled to receive analog signals and an output coupled to
4 the A/D converter;

5 providing an AGC control loop circuit coupled, in
6 feedback fashion, between the output of the A/D converter and the
7 AGC, the AGC control loop circuit receiving the digital signals
8 output by the A/D converter and generating a gain control signal in
9 operative response thereto; and

10 controlling the operation of the AGC circuit with the
11 gain control signal, such that the gain of the received analog
12 signals is regulated, in feedback fashion, in accordance with
13 regulated gain of the digital signals output by the A/D converter.

1 170. The method according to claim 167, wherein the multi-pair
2 bidirectional communication system comprises four unshielded
3 twisted wire pairs defining a local area network, the four pairs
4 further comprising a first pair adapted for signal transmission,
5 second and third pairs adapted for bidirectional signal
6 transmission and reception and a fourth pair adapted for reception,
7 the analog signals being received from at least one of the second,
8 third or fourth wire pairs, the method further comprising;

9 providing a automatic gain control (AGC) circuit having
10 an input coupled to receive analog signals and an output coupled to
11 the A/D converter;

12 providing an AGC control loop circuit coupled, in
13 feedback fashion, between the output of the A/D converter and the
14 AGC, the AGC control loop circuit receiving the digital signals
15 output by the A/D converter and generating a gain control signal in
16 operative response thereto; and

17 controlling the operation of the AGC circuit with the
18 gain control signal, such that the gain of the received analog
19 signals is regulated, in feedback fashion, in accordance with
20 regulated gain of the digital signals output by the A/D converter.